REMARKS

Favorable reconsideration of this application is respectfully requested in view of the following remarks. Claims 1-8 and 10-20 are pending in the present application, of which claims 1, 7 and 13 are independent. By virtue of this amendment, claim 9 has been canceled, and claims 1-4, 7, 10-11, 13 and 18-20 have been amended. No new matter has been added.

Claims 1-20 were rejected under 35 U.S.C. § 103(a) as allegedly being anticipated by Applicant's background ("the Background"), U.S. Patent No. 6,772,241 to George et al. ("George") and U.S. Patent No. 6,526,462 to Elabd.

Claim Rejection under 35 U.S.C. § 103

The test for determining if a claim is rendered obvious by one or more references for purposes of a rejection under 35 U.S.C. § 103 is set forth in MPEP § 706.02(j):

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Therefore, if the above-identified criteria are not met, then the cited reference(s) fails to render obvious the claimed invention and, thus, the claimed invention is distinguishable over the cited reference(s).

The Official action sets forth a rejection of claims 1-20 under 35 USC 103 (a) as being allegedly unpatentable over the Background of the present application, George and Elabd. This rejection is respectfully traversed for at least the following reasons.

Initially, it is respectfully submitted that the Background does not disclose or teach the subject matter of independent claims 1, 7 or 13. More specifically, the Background does not disclose

> multiple processors mounted on a single die; and
> multiple operating systems residing in a memory connected to said multiple processors,
> wherein each of said multiple processors executes an operating system of said multiple operating systems, and two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems,

as recited in claim 1;

> a plurality of processor groups mounted on a single die; and
> multiple operating systems residing in a memory connected to said groups,
> wherein each of said groups executes an operating system of said multiple operating systems, and two or more of said plurality of processor groups are capable of simultaneously executing two or more operating systems of said multiple operating systems,

as recited in claim 7; or

> processor means for executing a plurality of operating system means, wherein said processor means includes a plurality of processors mounted on a single die, and wherein said processor means is operable to simultaneously execute two or more operating system means of said plurality of operating system means,

as recited in claim 13.

The Background recites that Fig. 1 shows "a computer system 100 having multiple processors 10-40, each on a separate die (i.e., chip) 50-80, and connected to a single

operating system 90 stored in a memory 95." Page 1, lines 20-21. The Background does not describe the claimed multiprocessor system on a single die.

George discloses "a method of and apparatus for selective delivery of an interrupt to one of multiple processors having independent operating systems." Abstract. George further discloses a computer system 200 including a processor 210 and a co-processor 250. Col. 2, lines 55-61. The co-processor 250 is configured to operate with a mini OS. Col. 3, lines 12-14. The co-processor 250 is "configured as the master device" in the Limited ON mode and in the Listen mode, when the processor 210 is off. Col. 3, lines 28-34. Thus, the two processors are not simultaneously executing two or more operating systems in the Limited ON and the Listen modes since the processor 210 is off.

In the Full ON mode, "processor 210 may function as a master device with co-processor configured as a slave device." Col. 3, lines 35-37. Since the co-processor is configured as a slave device in the Full ON mode, the co-processor cannot execute an independent operating system in the Full ON mode. For instance, after a sleep event is detected, and a co-processor is determined to exist, the mini OS initializes. Col. 4, lines 23-35.

Thus, George does not teach or suggest a multiprocessing system in which "two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems," as recited in claim 1.

Further, George does not teach or suggest a multiprocessing system which comprises "a plurality of processor groups mounted on a single die" where "two or more of said plurality of processor groups are capable of simultaneously executing two or more operating systems of said multiple operating systems," as recited in claim 7.

Also, George does not teach or suggest a multiprocessing apparatus where a "processor means is operable to simultaneously execute two or more operating system means of said plurality of operating system means," as recited in claim 13.

The Examiner cites *In re Larson*, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965) to argue that "to make integral is not generally given patentable weight." Office Action, page 4, lines 3-4. In *In re Larson*, the prior art disclosed a brake disc and clamp comprised of "several parts rigidly secured together as a single unit." MPEP, 2144.04, V.B. The court in *In re Larson* held "that the use of a one piece construction instead of the structure disclosed in [the prior art] would be merely a matter of obvious engineering choice." *Id.* In the present case, neither the processors of the Background section nor the processors of George are disclosed to be rigidly secured together as a single unit.

Further, multiple processors cannot be merely integrated together. Thus, it would not be merely a matter of obvious engineering choice for a multiprocessing system to comprise "multiple processors mounted on a single die." Also, it would not merely be a matter of obvious engineering choice for a multiprocessing system to comprise "multiple processors mounted on a single die" where "each of said multiple processors executes an operating system of said multiple operating systems," as recited in claim 1. The Examiner has not recited any teaching or suggestion of such a combination.

The Examiner cites Elabd as evidence that an entire system "can be implemented or embedded on a single chip." Col. 1, lines 27-29. However, in the passage cited by the Examiner, Elabd does not discuss multiple operating systems. Thus, there is no teaching or suggestion in the Background, George or Elabd as to how to implement, for example, a multiprocessing system including multiple processors mounted on a single die "wherein each

of said multiple processors executes an operating system of said multiple operating systems, and two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems."

Further, none of the passages cited by the Examiner in the Background, George or Elabd teaches or suggests a multiprocessor system where "two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems," as recited in claim 1. Also, none of the cited passages teach or suggest a multiprocessing system where "two or more of said plurality of processor groups are capable of simultaneously executing two or more operating systems of said multiple operating systems," as recited in claim 7 or a multiprocessing apparatus where a "processor means is operable to simultaneously execute two or more operating system means of said plurality of operating system means," as recited in claim 13. Thus, any alleged combination of the Background, George and Elabd would not result in the subject matter recited in claims 1, 7 or 13.

As discussed above, claims 1, 7 and 13 are patentable over the Background, George and Elabd. Thus, claims 2-6, 8, 10-12 and 14-20, which depend from claims 1, 7 and 13, are also patentable over the Background, George and Elabd. These claims are also allowable over the references cited by the Examiner because cited references fail to teach or suggest the elements recited in these claims. For instance, with respect to claim 2, the cited references fail to teach or suggest that "at least one of said processors is operable to execute two or more of said multiple operating systems simultaneously."

Conclusion

In light of the foregoing, withdrawal of the rejections of record and allowance of this application are earnestly solicited.

Should the Examiner believe that a telephone conference with the undersigned would assist in resolving any issues pertaining to the allowability of the above-identified application, please contact the undersigned at the telephone number listed below. Please grant any required extensions of time and charge any fees due in connection with this request to deposit account no. 08-2025.

Respectfully submitted,

Stephen E. RICHARDSON et al.

Dated: November 24, 2004 By

Ashok Mannava
Registration No.: 45, 301

MANNAVA & KANG, P.C.
8221 Old Courthouse Road
Suite 104
Vienna, VA 22182
(703) 652-3822
(703) 991-1162 (fax)